EAST SEARCH

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L#	Hits	Search String	Databases
L1	442498	(digital or integrated) adj circuit$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	3839	1 and (("power supply" or "power distribution") adj (system$1 or unit$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	91	2 and ((("power supply" or "power distribution") adj (system$1 or unit$1)) same "voltage regula	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	54	2 and ((("power supply" or "power distribution") adj (system$1 or unit$1)) same (decoupling wi	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	8	3 and 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	6	2 and ((("power supply" or "power distribution") adj (system$1 or unit$1)) same "voltage regula	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	6	3 and slew	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L8	1691	((("power supply" or "power distribution") adj (system$1 or unit$1)) and "voltage regulator")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	392	((("power supply" or "power distribution") adj (system$1 or unit$1)) and (decoupling with (capacitor$1 or component$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	114	8 and 9	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	21	10 and simulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	9	10 and slew	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L14	0	8 and (cyclical with simulat$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L15	0	9 and (cyclical with simulat$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L16	9	8 and (cycle with simulat$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L17	1969	8 or 9	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L18	1	17 and "cycle simulation"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L19	0	17 and "cycle based simulation"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L20	0	17 and (cycle-by-cycle with simulat$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L21	4	17 and (cycles with simulat$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L23	11	22 and simulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L22	24	9 and ("bulk capacitance" or "total capacitance")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L24	0	2 and (cyclical with simulat$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L25	7	2 and (cycles with simulat$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L26	0	2 and "cycle based simulation"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L27	0	2 and (cycle-by-cycle with simulat$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L28	60	17 and "transient response"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L29	10	28 and simulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L30	298	17 and stability	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L32	3	31 and simulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L33	46	30 and simulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L31	27	28 and 30	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L35	2	34 and simulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L36	2	9 and 34	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

L34	26	((("power supply" or "power distribution") adj (system$1 or unit$1)) and "switching voltage regu	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

09/053140 **Donald Gay**

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Results of search set L10:(((digital or integrated) adj circuit$1) or "embedded systems") and (co-simulation or cosimulation) and (hardware adj simulator$1)

Document	Kind Codes	Title	Issue Date	Current OR	Abstract
US 20030105620	A1	System, method and article of manufacture for interface constructs in a programming languag	20030605	703/22	
US 20030074177	A1	System, method and article of manufacture for a simulator plug-in for co-simulation purposes	20030417	703/22	
US 20030046671	A1	System, method and article of manufacture for signal constructs in a programming language c	20030306	717/141	
US 20030046668	A1	System, method and article of manufacture for distributing IP cores	20030306	717/131	
US 20030037321	A1	System, method and article of manufacture for extensions in a programming lanauage capabl	20030220	717/149	
US 20030033594	A1	System, method and article of manufacture for parameterized expression libraries	20030213	717/141	
US 20030033588	A1	System, method and article of manufacture for using a library map to create and maintain IP c	20030213	717/107	
US 20030028864	A1	System, method and article of manufacture for successive compilations using incomplete para	20030206	717/141	
US 20020199173	A1	System, method and article of manufacture for a debugger capable of operating across multip	20021226	717/129	
US 20020152456	A1	Software and hardware simulation	20021017	717/135	
US 20020120909	A1	STATE MANAGEMENT IN A CO-VERIFICATION SYSTEM	20020829	716/5	
US 20020083420	A1	Method of co-simulating a digital circuit	20020627	717/135	
US 20020035464	A1	METHOD AND APPARATUS FOR GENERATING CO-SIMULATION AND PRODUCTION EX	20020321	703/22	
US 20020032559	A1	Hardware and software co-simulation including executing an analyzed user program	20020314	703/22	
US 20020019969	A1	Hardware and software co-simulation including simulating the cache of a target processor	20020214	716/5	
US 6470481	B2	State management in a co-verification system	20021022	716/5	
US 6298320	B1	System and method for testing an embedded microprocessor system containing physical and/	20011002	703/28	
US 6263302	B1	Hardware and software co-simulation including simulating the cache of a target processor	20010717	703/17	
US 6230114	B1	Hardware and software co-simulation including executing an analyzed user program	20010508	703/13	
US 6212489	B1	Optimizing hardware and software co-verification system	20010403	703/13	
US 6188975	B1	Programmatic use of software debugging to redirect hardware related operations to a hardwai	20010213	703/22	
US 5960191	A	Emulation system with time-multiplexed interconnect	19990928	703/28	
US 5946472	A	Apparatus and method for performing behavioral modeling in hardware emulation and simulat	19990831	703/6	
US 5838948	A	System and method for simulation of computer systems combining hardware and software int	19981117	703/27	
US 5771370	A	Method and apparatus for optimizing hardware and software co-simulation	19980623	703/13	
US 5768567	A	Optimizing hardware and software co-simulator	19980616	703/13	
US 5678028	A	Hardware-software debugger using simulation speed enhancing techniques including skipping	19971014	703/22	
US 5600579	A	Hardware simulation and design verification system and method	19970204	703/13	

US 5546562 A	Method and apparatus to emulate VLSI circuits within a logic simulator	19960813	703/14
US 20020032559 A	Co-simulation design system for testing electronic system, calculates time delay incurred by bl	20020314	